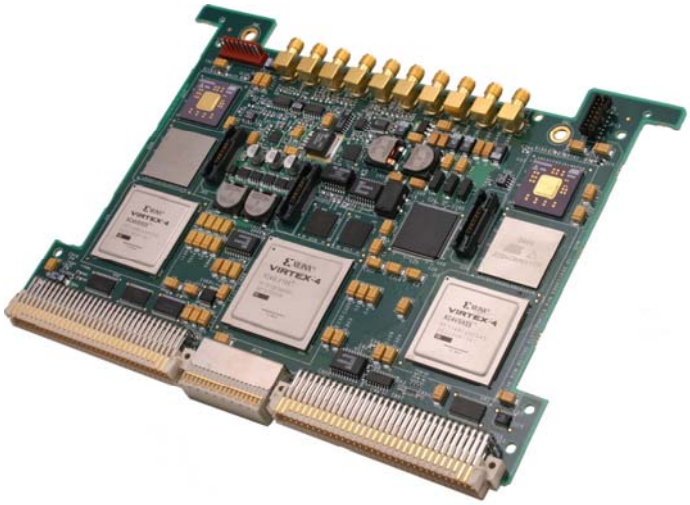
DUAL CHANNEL DIGITAL RECEIVER

RX 00103-008

Features

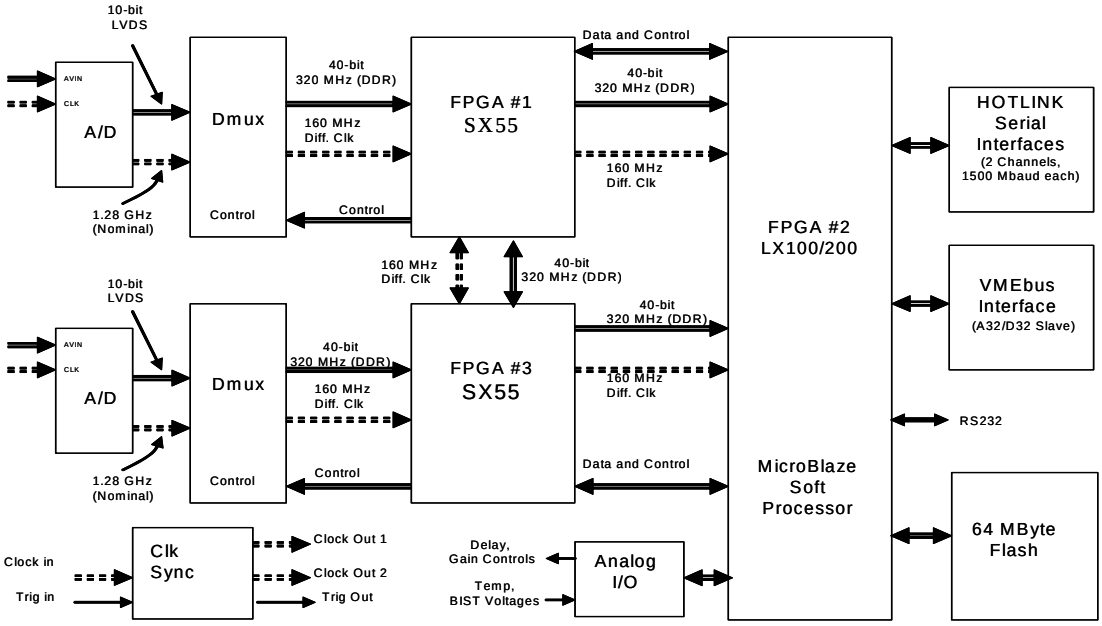
Dual Channel
Up to 2.2Gsps rate
Up to 3.3 GHz Analog
10 bit A/D
SFDR - 60dB typ. @ 1.6Gsps
SINAD - 47dB typ. @ 1.6Gsps
IMD - 60dB typ. @ 1.6Gsps
ENOB - 7.5 bits typ. @ 1.6Gsps
Sheltered Naval Environment
Conduction cooled (standard)
6U VME 64X
3 Virtex IV FPGAs



Applications

Digital Receiver
- Electronic warfare
- Radar
- Software Radio

High Speed Data Acquisition



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Description

The RX001003-008 is a 6U VME module that includes a dual channel high speed data acquisition board with standard conduction cooled heat-sink. (Pictured without heat-sink. It incorporates two AT84AS008 A/D converters and three Virtex IV FPGAs for signal acquisition/processing; two Hot-link serial 1500Mbaud interfaces; an 8 bit LVDS 320MHz DDR interface; and a VME 64x interface.

A/D

The board incorporates two AT84AS008 A/Ds from E2V. This device has a maximum sample rate of 2.2 Gsps at 10-bits with a 3.3 GHz full power input bandwidth. Device typical performance includes a spurious free dynamic range (SFDR) of -56 dBc and a SNR of 52 dBc for 7.8 effective bits at a sampling frequency of 1.7 Gsps and a signal frequency of 850 MHz. A companion device, the AT84CS001, de-multiplexes the high speed, 10-bit LVDS A/D outputs onto a 40-bit, LVDS bus running at 1/4 of the sample rate. The A/D's sampling delay and gain can be adjusted to support synchronizing and interleaving multiple A/D boards. The output of the de-multiplexer is connected to an SX55, Virtex-4 FPGA using the 40-bit LVDS bus and differential clock. This bus can operate at rates exceeding 500 MHz, supporting sample rates up to 2.2 Gsps.

FPGAs

The three Virtex-4 FPGAs include 2 SX55s, each connected directly to an A/D channel; the third site can be either an LX100 or LX200. The three FPGAs are interconnected with 40-bit, 400 MHz LVDS buses for array processing applications.

The FPGAs are also connected by an 80 MHz processor bus for lower speed communication; there are 17 address lines, 8 data lines and a number of control signals. A large number of spare I/O lines connect between each FPGA and the P2 connector for ancillary functionality and future expansion.

The LX100/200 (FPGA #2 in Figure 2) typically contains the Microblaze soft-processor, the Hotlink, VME P0, and VME 64x interfaces.

CPU

FPGA#2 can be configured with the Microblaze soft processor. This is a 32-bit RISC processor that is used for programming Flash, local control, and built-in test. In a typical configuration, it utilizes less than 10% of the LX100's resources. The processor is highly configurable; memory and peripherals are easily added or removed depending on the application. This module also provides an RS232 interface commonly used for applications such as Labview .

CPLD and Flash Memory

There are 64 megabytes of Flash memory that can be used to store multiple FPGA configurations and user data. At power-up, a XCR3164 CPLD loads the FPGAs using the 8-bit select-Map mode; after power-up, the CPU can read and write Flash, storing user data or updating the FPGA configurations. The FPGAs can also be re-configured on-the-fly using the multiple FPGA configurations.

Hotlink Interface

High speed serial links are implemented using the CYP15G0101DXA HOT-Link II™ Transceiver from Cypress Semiconductor. It contains the logic to support the SERDES function and clock recovery and supports data rates from 200-1500 Mbaud. FPGA#2 acts as the system host to the device; data can be written to or read from the device using a dual port memory bank within the FPGA. Drivers supporting the serial front panel data port protocol (VITA 17.1) can be provided. The physical interface is single-ended copper (MCX).

VME Interface

The VME bus interface is designed to conform to the VME64x specification and requires the 160 pin connectors with the added ground pins and +3.3 volt power pins. The interface is designed to support A32/D32 slave data transfers directly to and from a dual port memory buffer residing in FPGA#2. The logic required for the VME bus protocol is resident in the FPGA; external transceivers are used to buffer the VME bus signals.

Power

Power is supplied through the VME backplane. Special power supply voltages, that are not part of the VME specification, are supplied through user defined pins on the P2 connector. These pins supply core voltages to the FPGAs of 2.5V (directly), and 1.2V (via an ob-board DC-DC converter.

Clock Synchronization

The sampling clock input is single ended or differential, AC coupled. The input clock is buffered and distributed to each A/D channel, and to the front panel for synchronization of multiple boards. The clock can also be stopped and started by the CPU, glitch-free, to synchronize each channel. That is, the clock can be stopped, the A/Ds and de-multiplexers reset, and then the clock restarted to ensure that the samples across all channels are aligned in time.

Additional Capabilities

LNX can support the development of custom algorithms for specific applications. We have the expertise and tools in house for algorithm development and FPGA logic optimization. Our tools allow us to develop and simulate fixed-point DSP algorithms in Matlab™ and automatically convert those algorithms into VHDL for synthesis and implementation on the FPGAs. This allows us to rapidly develop, simulate, and test new algorithms without having to manual convert new

algorithms to VHDL or Verilog. With the tools and capabilities we have in house, we can also tailor the design as necessary to implement new requirements.

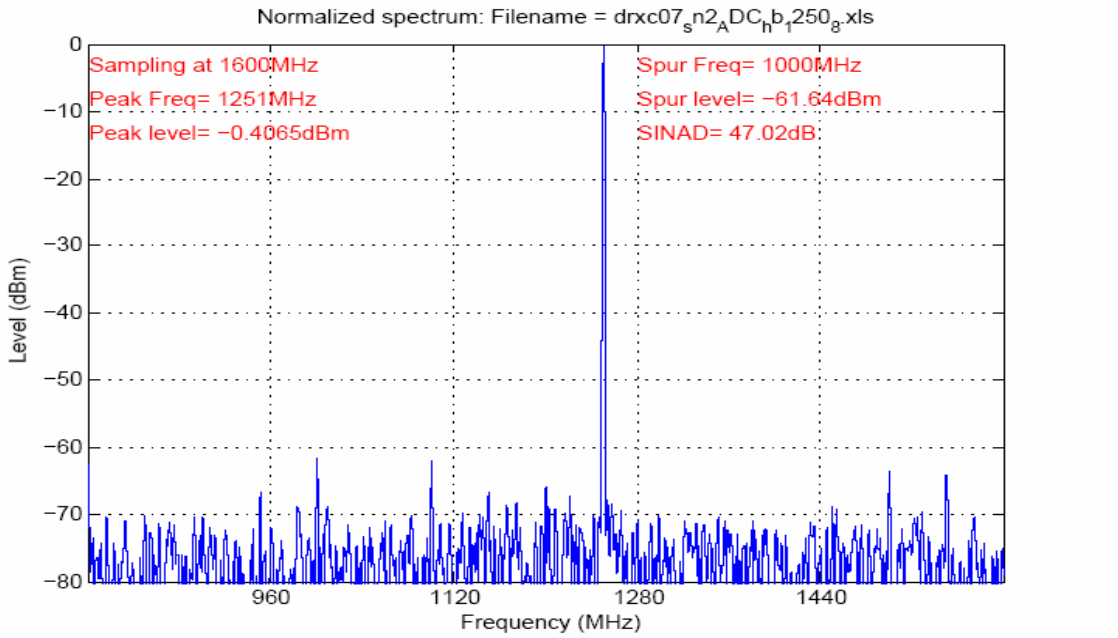

Figure1. Example SFDR/SINAD

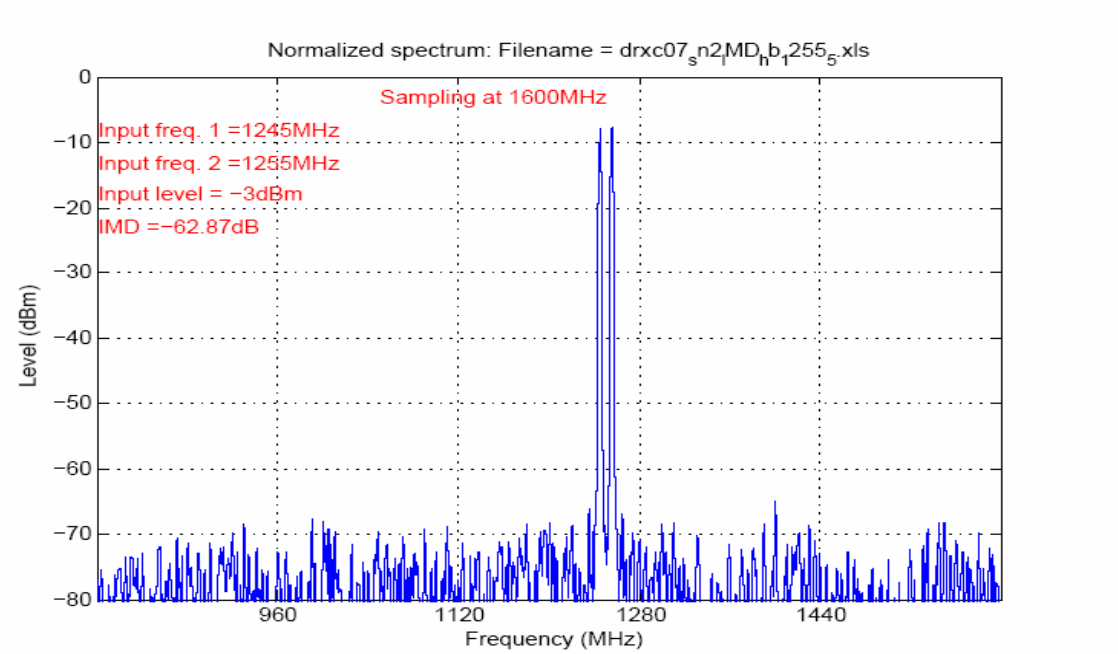

Figure2. Example IMD Performance

Specifications

High Speed Interfaces

Analog Inputs (2 Channels)
Type: Differential or Single Ended
Impedance: 50 ohm
Connectors: MCX
Max Power Level: -2dBm
Frequency range: DC-3.3GHz

Sample Clock Input
Type: Differential or Single Ended, AC coupled
Square-wave or Sine-wave
Impedance: 50 ohm
Connectors: MCX
Power Level Range 10dBm to -10dBm
Frequency range: 100MHz to 2.2GHz

Sample Clock Output
Type: Differential, AC coupled
Square-wave
Impedance: 50 ohm
Connectors: MCX
Output level: 600mV P-P typical
Frequency range: 100MHz to 2.2GHz

Hot-Link Outputs (2 channels)
Type: Single ended, transformer coupled
Impedance: 50 ohm
Connector: MCX
Output level: 600mV P-P typical
200-1500 Mbaud

VME Interfaces

VME 64x
Dual Port Memory
Address: 32
Data: 32

VME P0
Type: Differential
Impedance: 100 ohm
Level: Standard LVDS
Signals: 8 Data, Clock
Speed: 320MHz DDR

Power Supplies

Location: VME backplane

Voltage	Current maximum
+28V+/-5%	1.2A*
+5V+/-5%	500mA
+3.3V+5%/-2.5%	3.5A
+2.5V+/-5%	3.5A
-5V+/-5%	2.5A

*The power supply requirements for the +28V are dependent on the number of gates used and the processing clock frequency in the FPGAs.

FPGAs

XILINX, XC4VSX55 (2 channels)
Primary Functions: A/D interface, Signal Processing, Processor interface
55K Logic Cells
384 Kb distributed RAM
5.76 Mb Block RAM
500MHz Xtreme DSP slices

XILINX, XC4VLX100
Primary Functions: Micro-blaze Processor, Interface to Signal Processing FPGAs, data processing, VME and serial interfaces
110K Logic Cells
768 Kb distributed RAM
4.32 Mb Block RAM
500MHz Xtreme DSP slices

Environmental

Weight: .78Kg
Storage temperature: -40C to 100C
Operating temperature: -20C to 70C
Conduction cooled – 0C-70C cold plate (standard) – consult factory for other cooling configurations, storage, and operating temperature ranges)
Vibration, 2-100 Hz, 0.8g
Shock, half sine, 10g, 50 ms
Salt fog, humidity (MIL-STD-810F)