Monobit Digital Instantaneous-Frequency-Measurement Module

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Abstract: In conventional Electronic Warfare (EW) or Electronic Countermeasure (ECM) systems, Instantaneous Frequency Measurement (IFM) receivers are used to sense the frequency of a radar pulse in real time. However, due to the architectures of these systems, it is difficult to measure two simultaneous frequencies. An emerging solution, the Monobit Receiver, was developed to address this issue. A monobit receiver is a single-bit analog to digital converter, plus advanced digital signal processing (DSP) algorithms to extract the frequency and phase information. Key enabling technologies for monobit receivers include monobit analog-to-digital conversion (ADC), high speed demultiplexing, and digital processing. We will review an example of a monobit receiver design and discuss some of its capabilities and characteristics.

Introduction

In conventional Electronic Warfare (EW) or Electronic Countermeasure (ECM) systems, Instantaneous Frequency Measurement (IFM) receivers are used to make real time measurements of key characteristics of a radar pulse, such as frequency, amplitude, and pulse width. However, due to the inherent limitations of their architectures, these IFM systems cannot measure simultaneous signals that overlap in time. An emerging solution, the *monobit receiver*, was developed to address this issue. A monobit receiver is a system that includes RF signal shaping and filtering functions, a single-bit analog to digital converter, a demultiplexer to interface the high speed digital data to commercially available FPGAs, and advanced digital signal processing (DSP) algorithms to extract the frequency and phase information.

Several companies have developed monobit receiver designs. In this article, we will review the critical components of a monobit receiver, and discuss a design example and some of its capabilities and characteristics.

Critical Components of a Monobit Receiver

The high speed monobit analog to digital converter is the key enabler of the monobit receiver design. Its function is to accurately digitize the input signal at the correct times. Two of the key specs for the monobit ADC are the input analog bandwidth and the thermal offset voltage. The input analog bandwidth determines the maximum signal frequency that can be sampled; this is important in a bandpass sampling configuration, where the signal frequency can be greater than the sample frequency. The thermal offset voltage is analogous to the input hysteresis for high-speed measurements. In the monobit receiver application, where the monobit ADC must make accurate decisions relative to a threshold voltage for input signals that have varying histories in the time domain, it is important to minimize the dependency of the threshold voltage on past signal conditions. Such variations of the threshold voltage can be thought of as a thermal offset voltage, as the threshold voltage is shifted by thermal asymmetries that result from the electrical asymmetries in the differential data path in the monobit ADC. This thermal offset voltage is input data dependent, and is typically more significant than the DC hysteresis.

The output from the monobit ADC is a high-speed digital signal at many gigabits per second. In order to interface this to commercially available FPGAs which generally have LVDS I/O at up to 1 or 2 Gbps, a high speed demultiplexer is needed to deserialize the high-speed bit stream into parallel lanes at lower speed. For example, a 10 Gbps high-speed bit stream can be demultiplexed by a 1:8 demux, to interface to a FPGA at 1.25 Gbps.

The single bit digitization in a monobit receiver enables sampling at very high speeds. However, the accompanying trade-off is that by quantizing to only one bit, a large number of spurious frequencies are generated. Therefore, digital signal processing is required to resolve between the real signal frequencies and the spurious frequencies, via thresholding or other techniques. An additional requirement is to perform this signal processing in real time, within the power constraints of the system.

Design example of a monobit receiver prototype

We now review a design example of a monobit receiver from LNX Corporation, for frequency measurement over the 0.5 – 18 GHz band. A block diagram appears in *Figure 1*; specifications appear in *Table 1*.

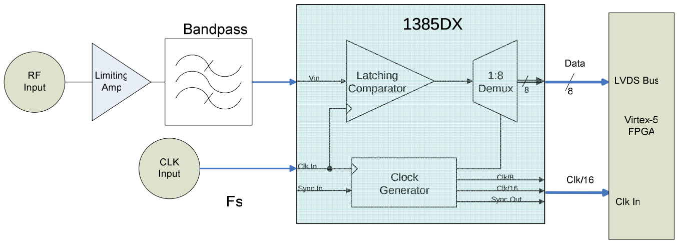

Figure 1. Monobit Receiver Block Diagram

Parameter	Performance
Operating Frequency Range:	2 to 18.0 GHz
Frequency Resolution:	1.0 MHz (extend to 0.5 MHz)
Number of Data Bits:	14 (extend to 15)
Throughput Time (normal throughput):	200 nanoseconds
Dynamic Range:	-50 to +10 dBm
RF Input Signal-to-Noise Ratio:	0 db (With 99% Valid Rate)
Frequency Error (RMS) at 0 dB S/N:	3.0 MHz (Valid Data Only)
RF Input Pulse Width:	50 ns to CW
RF Input VSWR:	2.2:1 maximum
Temperature Range:	-40ºC to +85ºC
Size:	6.5” by 5.4” by 2”
Weight:	3 pounds maximum

Table 1. Monobit Receiver Key Characteristics

System Description

The LNX Monobit DIFM (Digital Instantaneous Frequency Measurement) is based on a very high speed monobit ADC. Multiple channels are required to cover the full 0.5 to 18 GHz band; however, the LNX design uses band pass sampling techniques, or direct digital down conversion to eliminate intermediate, mixer based down conversions. All of the digital processing is performed in a single FPGA.

RF Front End

Limiting Amplifier

The limiting amplifier has an operating bandwidth of 0.5-18 GHz. The loss of the frequency multiplexer including the power divider and filters will be approximately 12 dB; the power output of the limiting amplifier is > +10 dBm.

Frequency Multiplexer

The partitioning of the 0.5-18 GHz frequency spectrum depends on the maximum sample rate allowed by the digitizer coupled with the ability to handle the demultiplexed data rate.

Digitization and Demultiplexing

The high-speed digitization is performed using the Inphi 1385DX 12.5 Gbps 1:8 demultiplexer, which has a high-sensitivity latched comparator front end with an analog bandwidth greater than 14 GHz. The 1:8 demultiplexer can operate at rates up to 12.5 Gbps.

The input amplitude to the demultiplexer is 500 mVpp (-2dBm). This sets the output power requirement of the limiting amplifier. The demultiplexer provides a demultiplexed 8-bit value and $F_s/16$ data clock. For example, if the clock/sample rate for each channel is 8.192 GHz, then the data rate after demultiplexing is 1.024 Gbps. The clock is aligned such that clock transitions occur in the middle of data transitions, simplifying clocking at the destination.

Digital Processing

There are a number of different processing techniques that can be used to perform the frequency measurement. We will review FFT processing and delta phase processing.

FFT Processing

A significant advantage of the monobit receiver is its ability to process simultaneous signals. A technique such as the Fast Fourier Transform can be used to exploit this. *Figure 2* shows the results for two tones separated by 90 MHz sampled at 10 Gsa/s. Each peak is clearly discernable. However, there are some disadvantages.

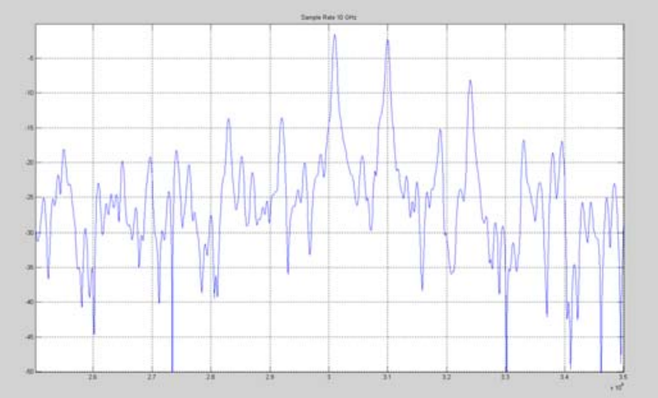

Figure 2. FFT processing result for two input signals at 3.01 GHz and 3.10 GHZ (90 MHz separation), sampled at 10 Gsa/s

First, the FFT algorithm is computationally intensive, especially for long data frames. Data must be processed as blocks or frames of data; it may be advantageous to overlap the data frames in time, but this increases the amount of processing required. However, because the raw data consists of a single bit, a zero or a one, many operations are trivial multiplications by a 0 or 1.

Second, the frequency resolution of the FFT is determined by the sampling rate and number of samples, or Fsample/no_of_points. For example, a 100 nanosecond record, sampled at 10 Gsa/s, will have 1000 points and a frequency bin spacing of 10 MHz.

Delta Phase Processing

Another technique to measure frequency is based on a delta phase calculation. This technique is not as computationally intensive, but it does not perform well with simultaneous signals. The frequency is measured by determining $\delta\phi/\delta t$.

Phase values are generated from the amplitude values by a number of steps. For example, bandpass filtering and sampling translates an Fs/2 block of spectrum to the first Nyquist zone from 0 to Fs/2. The data is multiplied by a complex multiplier to shift the spectrum from –Fs/4 to +Fs/4. The data is converted to a complex representation with in-phase and quadrature components. The conventional way to generate in-phase and quadrature components from a real signal is to do a Hilbert transform; the complex multiplication eliminates the need to do it as a separate step.

The phase is calculated by taking the arctangent of the in-phase and quadrature components using a look up table. Finally, delta phase is calculated by taking the phase difference between successive samples. The delta phase values can be averaged over a period of time (such as an input pulse width) in order to improve the accuracy.

Processing Results

Data was collected at a variety of sample rates, input frequencies, and signal to noise ratios, and analyzed and processed using both FFT and delta phase processing techniques. The steps for delta phase processing were as follows:

1. The data was multiplied by a complex signal at $F_s/4$. For an input band from 500 to 2500 MHz, after multiplication, the band extends from -1545.5 to +454.5 MHz. As seen in *Figure 3*, the band is asymmetric with respect to DC because of the sample rate used (8.1818 GHz) and the desire to multiply by $F_s/4$.

2. After low pass filtering, the complex data (I/Q) data is converted to amplitude and phase and a delta phase calculation is performed. Finally, the average delta phase value is converted to frequency using the formula freq = ((avg_delta_phi * fsample) / (2 * pi) – (fsample / 4).

The results are summarized in *Tables 2 and 3*, which show that both the FFT processing method and the "Freq Estimate" yielded by the delta phase processing method accurately measure the signal frequency.

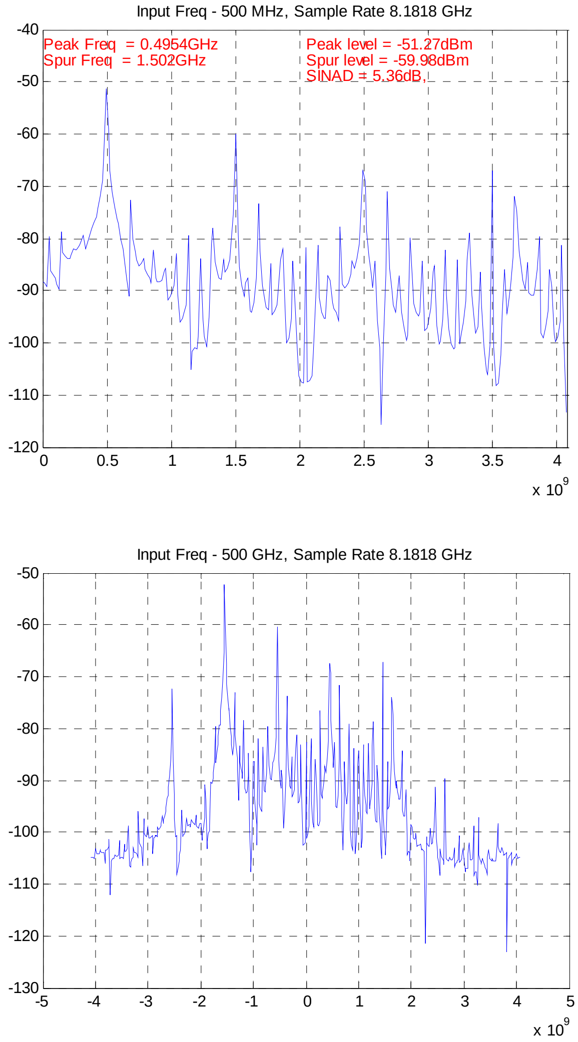

Figure 3. Real FFT of original input signal at 500 MHz and the output after a complex frequency shift and filtering.

Sample rate	Input Freq (MHz)	FFT Peak (GHz)	Delta Phase (pi radians)	Delta Phase Freq Estimate (GHz)	Delta Phase Freq Error (MHz)
8.18E+09	500	0.4954	1.1879	0.4986	1.4272
8.18E+09	900	0.8949	0.8810	0.8982	1.8104
8.18E+09	1300	1.2944	0.5710	1.3019	1.9231
8.18E+09	1700	1.6939	0.2656	1.6996	0.4264
8.18E+09	2100	2.0934	-0.0437	2.1023	2.2934
8.18E+09	2400	2.3970	-0.2719	2.3995	0.5024

Table 2. Comparison of results from FFT and delta phase algorithms, sampled at 8.1818 Gsa/s

Sample Rate	S/N	Input Freq (MHz)	FFT Peak (GHz)	Delta Phase (pi radians)	Delta Phase Freq Estimate (GHz)	Delta Phase Freq Error (MHz)
1E+10	5	3000	3.0078	-0.3059	2.9869	13.1467
1E+10	3	3000	3.0078	-0.3078	2.9899	10.0746
1E+10	1	3000	3.0078	-0.3074	2.9893	10.7179
1E+10	0	3000	3.0078	-0.3054	2.9860	14.0120

Table 3. Data collected with varying SNR, sampled at 10 Gsa/s,

Conclusion

Monobit receivers are a promising emerging solution for measuring simultaneous frequencies of radar pulses in real time. The critical elements of a monobit receiver system are the single-bit analog to digital converter, the demultiplexer to interface the high speed digital data to commercially available FPGAs, and advanced digital signal processing (DSP) algorithms to extract the frequency and phase information. We reviewed a prototype monobit receiver design from LNX and discussed the processing results.